Confirmation No.8503

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	ROOZEBOOM *et al.*	Examiner:	Chen, David Z.
Serial No.:	10/560,717	Group Art Unit:	2815
Filed:	December 15, 2005	Docket No.:	NL040226US1 (NXPS.351PA)
Title:	ELECTRONIC DEVICE, ASSEMBLY AND METHODS OF MANUFACTURING AN ELECTRONIC DEVICE		

APPEAL BRIEF

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P.O. Box 1450
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Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed December 18, 2009 and in response to the rejections of claims 1-10 and 20-27 as set forth in the Final Office Action dated September 18, 2009.

Please charge Deposit Account number 50-4019 (NL040226US1) $540.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

I. Real Party In Interest

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

II. Related Appeals and Interferences

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

III. Status of Claims

Claims 1-10 and 20-27 stand rejected and are presented for appeal. Claims 11-19 are cancelled. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action dated September 18, 2009.

V. Summary of Claimed Subject Matter

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to an electronic device comprising a semiconductor substrate having a

first side and a second side (*see, e.g.*, Figures 4a-4e, reference numbers 1 and 2). The electronic device having a vertical trench capacitor on the first side of the substrate (*see e.g.*, Figure 4b, reference number 21), the vertical trench capacitor including a plurality of trenches in which dielectric material is present between first and second conductive surfaces (*see, e.g.*, Figure 2c, reference 11 and page 11:15-19); and a vertical interconnect that extends through the substrate from the first side to the second side (*see, e.g.*, Fig. 2c, reference 30), the vertical interconnect being insulated from the substrate by dielectric material (*see, e.g.*, Fig. 2c, reference 30 and reference 11), the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer (*see, e.g.*, Figure 2c and page 2: 30-34).

Commensurate with independent claim 22, an example embodiment of the present invention is directed to an electronic device comprising: a semiconductor substrate having a first side and a second side (*see, e.g.*, Figures 4a-4e, reference numbers 1 and 2); a plurality of trenches on the first side of the substrate (*see, e.g.*, Figure 4b, reference number 21), each of the trenches extending into the substrate from the first side (*see, e.g.*, *id.*); conductive material lining each of the trenches (*see, e.g.*, Figure 2b, reference 22 and page 10, 31-33); a vertical interconnect that extends through the substrate from the first side to the second side (*see, e.g.*, Figure 2c, reference 30), the vertical interconnect having walls (*see, e.g.*, *id.*); a single deposition layer of dielectric material on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect (*see, e.g.*, Figure 2c and page 2:30-34).

VI. Grounds of Rejection to be Reviewed Upon Appeal

The grounds of rejection to be reviewed on appeal are as follows:

A. Claims 1, 5-8, 10, 20-23 and 27 stand rejected under 35 U.S.C. § 103(a) over Chudzik (U.S. Patent No. 7,030,481) in view of Dhong (U.S. Patent No. 6,221,769).

B. Claims 2-4 and 24-26 stand rejected under 35 U.S.C. § 103(a) over the '481 and '769 references and further in view of Hsuan (U.S. Patent Pub. 2001/0005046).

C. Claim 9 stands rejected under 35 U.S.C. § 103(a) over the '481 and '769 references in view of Sakai (U.S. Patent No. 5,872,393).

VII. Argument

Generally, the § 103 rejections fail to establish correspondence to the claimed invention, and aspects of the cited references teach away from the assertions made in the (final) Office Action. The Examiner improperly categorizes one of the claim limitations (*e.g.*, "single deposition layer") present in all of the claims as a "product by process" limitation, ignoring the distinctive structural characteristics of the final product. In ignoring the limitation the Examiner has failed to provide correspondence to certain aspects of the claimed invention. Accordingly, Appellant believes that all rejections are improper for failing to establish correspondence to the claimed invention. The following addresses the characterization of certain claim limitations as "product by process" in greater detail, as well as the lack of correspondence, and the impropriety of the § 103 rejections in view of the lack of motivation/teaching away in the references themselves.

A. The § 103(a) Rejection Of Claims 1, 5-8, 10, 20-23 And 27 Is Improper.

1. The § 103(a) Rejection Is Improper Because The Cited References Teach Away From The Proposed Combination.

Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('481) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (U.S. 2007). ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious.") *See, also In re Gordon*, 733 F.2d 9-00 (Fed. Cir. 1984) (A § 103 rejection cannot be maintained when the asserted modification undermines the purpose of the main reference). In this instance, the '481 reference explicitly teaches away from the combination with the '769 reference as asserted (to form a common dielectric layer). Specifically, the '481 reference acknowledges the method of manufacture of vertical interconnects described in the '769 reference (Col. 4:16-17), but requires that the

corresponding dielectric layer be separate (and is formed in a separate, not common, step) *See* Col. 5:60-Col. 6:12. The proposed combination and the disclosed approach in the '769 reference thus is not and cannot be combined with the '481 reference to correspond to a single layer of common material as claimed.

In addition, as the issues the Office Action relies upon as alleged motivation are expressly addressed by the '481 reference, the asserted combination proposes a process that would not be implemented because it would both increase costs and attempt to implement an electronic device with improper/unusable layers. The '481 reference explains that the material 3020 is a hi-K dielectric material (Col. 5:11-16) which requires special high temperature processing steps and tools to deposit it in the vertical trenches, which are incompatible with the conductors employed in the vias, and further explains that the hi-K material should be processed first in order to keep the costs at a minimum. *See* Col 5:66 *et seq.*

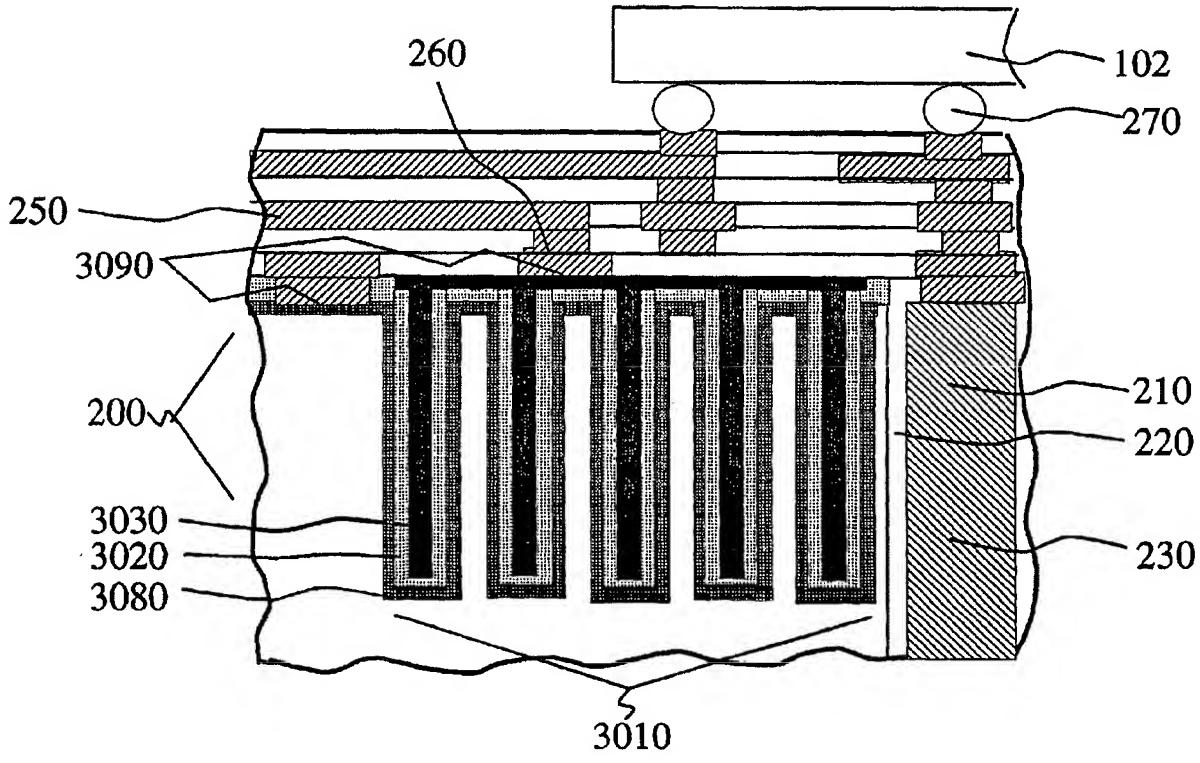
Under M.P.E.P. § 2143.01 and the above-cited *KSR* and *In re Gordon* decisions, the rejection should be reversed.

2. <u>The Asserted Combination Of References Lacks Correspondence.</u>

The § 103(a) rejection of claims 1, 5-8, 10, 20-23 and 27 is improper because the cited '481 reference, either alone or in combination with the '769 reference, lacks correspondence. For example, neither of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.*, a single layer of dielectric material that extends into both vertical capacitor trenches and vias. In contrast, the Office Action (at page 3) acknowledges that the '481 reference does not specifically disclose a vertical trench capacitor and a vertical interconnect sharing a common dielectric material formed from a single deposition layer. The '769 reference fails to overcome this lack of disclosure. The '769 reference discloses using the asserted dielectric material exclusively in vias. As a further example, the '481 reference explicitly recites that capacitor and via dielectric materials are different, explaining that the capacitor dielectric material requires special steps and tools that are incompatible with the conductive material of the interconnect layers. *See* Col. 5:66-Col. 6:3. In the Advisory Action, the Examiner attempts to provide

correspondence to the single dielectric layer of common dielectric material (leaving aside the requirement for a single deposition layer for a moment) by citing to Fig. 3b and the fact that "the '481 reference specifically discloses a commonly owned patent, which is the '769 reference." However, Fig. 3b (reproduced below) clearly shows that the dielectric 3020 of the vertical trenches is made of a separate material than the insulator 220 used in the through vias 210 and between the interconnect vias 260. Additionally, even though the '481 reference acknowledges the teachings of the '769 reference, the '481 reference fails to teach the hypothetical combination presented by the Examiner. Therefore, the proposed combination fails to disclose, teach or suggest a common dielectric layer for both the trenches and the through vias as asserted. Because the hypothetical combination fails to provide

Figure 3b.



correspondence to the claimed invention, the rejection of claims 1, 5-8, 20-23 and 27 must fail. Appellant requests the rejection be reversed.

3. The Office Action Erroneously Characterizes Certain Limitations As A "Product By Process" Step Not Requiring The Office Action To Establish Correspondence.

Appellant traverses the Examiner's characterization of the claim limitations directed to a single deposition layer as a product by process limitation that does not structurally distinguish the claimed invention over the prior art. In characterizing the limitations as a product by process step the Examiner has ignored the limitations. Under M.P.E.P. § 2113, when the structure implied by the process steps would be expected to impart distinctive structural characteristics to the final product, the relevant limitations cannot be ignored. *See, e.g., In re Garnero*, 412 F.2d 276, 279 (CCPA 1979). As applied to the instant claim language the Examiner is attempting to ignore that the "single deposition layer" provides relevant distinctive structural characteristics in the final product. The Examiner's position is contrary to the requirements of M.P.E.P. § 2113.

The record supports the Appellant's position that a single deposition layer provides relevant distinctive structural characteristics. The single deposition layer overcomes problems pointed out and discussed in Appellant's specification at page 2, lines 20-29. The specification goes on to say that one insight is that both the vertical capacitors and the vertical interconnects are processed simultaneously to provide certain structural/electrical advantages. *See* Appellant's specification page 2, lines 30-34. (The Examiner is not considering the invention "as a whole" (§ 103(a)) when the "single deposition layer" limitation is ignored.) Moreover, Appellant further discuses multiple layers ("couple of layers") as separate and distinguishable from a single layer deposited by a "common" step (*e.g.*, figures 2c, 4b and 4c further illustrate and provide related discussion of a single deposition in contrast to multiple layers). Additionally, such structural characteristics are discussed (and therefore would be appreciated by the skilled artisan) with respect to Fig. 3A and 3B of the '481 reference, where, for example, atomic layer deposition (ALD) and chemical vapor deposition (CVD) are used to provide conformality, and where multiple examples of dual deposition layer materials provide entirely different structural and electrical

characteristics (Col. 5:1-28 of '481 reference). Similarly, in connection with the asserted '769 reference, single and dual formed deposition layers are discussed in connection with problems and proposed solutions thereof. In the preferred embodiment of Fig. 2 of the '769 reference, single deposition barrier layer 203 (deposited by CVD) is taught as being useful as a protective material mitigating reaction between the conductive layer and the silicon layer which can be highly reactive with other metal materials. Further, the '769 reference explains that "those skilled in the art are familiar with the processes involved" for depositing and forming such layers (Col. 6: 32-35 of '769 reference). Appellant respectfully submits that these are but two examples of un-rebutted evidence that one of skill in the art would readily recognize physical manifestations ensuing from a single deposition process step. Therefore, Under M.P.E.P. § 2113, the Examiner cannot ignore the claim limitations regarding a "single deposition layer."

Moreover, the use of such language is a common practice sanctioned by the USPTO. A search of the USPTO issued patent database results in a long list of patents having such apparatus claims with such (§ 2113) structural-type characteristics and the same or similar claim terminology ("layer" and "single deposition"). *See*, for example, 6,815,825 ("a layer of hard mask material formed by a single deposition"); 7,505,722 ("and the wiring layer are formed by a single deposition step"); 7,569,915 ("formed from a single deposition layer"); and 7,116,124 ("constructed over a surface of the probe card during a single deposition").

Referring to the rejection of claim 23 as an example, the Office Action has improperly construed the limitation "a single deposition layer of dielectric material" as involving a process step. This erroneous interpretation is inconsistent with the claim, which is directed to a single layer of material "on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect." That this layer was formed in a single deposition characterizes the layer, but does not permit the Examiner to ignore limitations directed to a single layer of common material. Accordingly, by ignoring these limitations as process steps the Office Action has failed to show correspondence to the claimed single layer of common material. Therefore the § 103 rejection is improper and Appellant requests that it be reversed.

B. The § 103(a) Rejection Of Claims 2-4 And 24-26 Is Improper.

The § 103 rejection of claims 2-4 and 24-26 is improper because the cited combination of the '481 reference and the '769 reference does not correspond to the claimed invention as discussed above under heading A(2). Moreover the '481 reference teaches away from the Examiner's proposed combination as discussed under heading A(1). Appellant notes that the '046 reference is not alleged by the Examiner to address the above discussed deficiencies of the cited combination of the '481 reference and the '769 reference. For at least these reasons, the § 103 rejection of claims 2-4 and 24-26 is improper since they depend from independent claims 1 and 23.

In view of the above, Appellant requests that the § 103 rejection of claims 2-4 and 24-26 be reversed.

C. The § 103(a) Rejection Of Claim 9 Is Improper.

The § 103 rejection of claim 9 is improper because the cited combination of the '481 reference and the '769 reference does not correspond to the claimed invention as discussed under heading A(2). Moreover, the '481 reference teaches away from the proposed combination as discussed above under heading A(1). Appellant notes that the '046 reference is not alleged by the Examiner to address the above discussed deficiencies of the cited combination of the '481 and '769 references. For at least these reasons, the § 103 rejection of claim 9 is improper since it depends from claim 1.

In view of the above, Appellant requests that the § 103 rejection of claim 1 be reversed.

APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/560,717)

1. An electronic device comprising a semiconductor substrate having a first side and a second side; a vertical trench capacitor on the first side of the substrate, the vertical trench capacitor including a plurality of trenches in which dielectric material is present between first and second conductive surfaces; and a vertical interconnect that extends through the substrate from the first side to the second side, the vertical interconnect being insulated from the substrate by dielectric material, the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer.

2. An electronic device as claimed in Claim 1, wherein the vertical interconnect has a first part and a second part, which first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape.

3. An electronic device as claimed in Claim 1, characterized in that the vertical interconnect includes a plurality of parallel trenches each of which is substantially filled with electrically conductive material.

4. An electronic device as claimed in Claim 2, characterized in that the first part of the vertical interconnect comprises a plurality of parallel through-holes that extend from the first side of the substrate to the second part of the vertical interconnect, each of the plurality of parallel through-holes being substantially filled with electrically conductive material.

5. An electronic device as claimed in Claim 1, characterized in that:
- contact pads for coupling to an external carrier are present on the second side;
- a first vertical interconnect is used for grounding and
- a second interconnect is used for signal transmission.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-10 and 20-27 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

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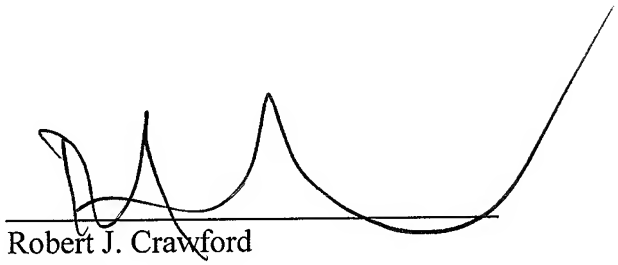
By: 

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APPENDIX OF CLAIMS INVOLVED IN THE APPEAL
(S/N 10/560,717)

1. An electronic device comprising a semiconductor substrate having a first side and a second side; a vertical trench capacitor on the first side of the substrate, the vertical trench capacitor including a plurality of trenches in which dielectric material is present between first and second conductive surfaces; and a vertical interconnect that extends through the substrate from the first side to the second side, the vertical interconnect being insulated from the substrate by dielectric material, the dielectric material of the vertical interconnect and the dielectric material of the vertical trench capacitor being common material formed from a single deposition layer.

2. An electronic device as claimed in Claim 1, wherein the vertical interconnect has a first part and a second part, which first part is exposed on the first side of the substrate, is narrower than the second part and has a substantially cylindrical shape.

3. An electronic device as claimed in Claim 1, characterized in that the vertical interconnect includes a plurality of parallel trenches each of which is substantially filled with electrically conductive material.

4. An electronic device as claimed in Claim 2, characterized in that the first part of the vertical interconnect comprises a plurality of parallel through-holes that extend from the first side of the substrate to the second part of the vertical interconnect, each of the plurality of parallel through-holes being substantially filled with electrically conductive material.

5. An electronic device as claimed in Claim 1, characterized in that:
- contact pads for coupling to an external carrier are present on the second side;
- a first vertical interconnect is used for grounding and
- a second interconnect is used for signal transmission.

6. An electronic device as claimed in Claim 5, characterized in that the first and second vertical interconnect are designed so as to form a coaxial structure.

7. An electronic device as claimed in Claim 1, characterized in that an integrated circuit is defined on the second side of the substrate.

8. An electronic device as claimed in Claim 1, characterized in that the substrate comprises a high-ohmic zone which is present adjacent to the vertical capacitors and acts as a protection against parasitic currents.

9. An electronic device as claimed in Claim 8, further comprising a planar capacitor on the first side of the substrate, the planar capacitor including dielectric material formed from common material of the single deposition layer, and wherein the high-ohmic zone separates the planar capacitor from the vertical trench capacitor.

10. An assembly comprising the electronic device of claim 1, and a semiconductor device, which semiconductor device is electrically connected to bond pads present on the first side of the substrate.

20. An electronic device as claimed in claim 1, wherein the dielectric material of the vertical trench capacitor and the dielectric material of the vertical interconnect are formed by depositing a layer of dielectric material on the substrate and partially etching the deposited layer of dielectric material.

21. An electronic device as claimed in claim 1, wherein the dielectric material of the vertical trench capacitor and the dielectric material of the vertical interconnect are identical dielectric material formed from the single deposition layer.

22. An electronic device as claimed in claim 1, wherein the vertical interconnect is substantially filled with conductive material, the conductive material of the vertical

interconnect and the second conductive surface of the vertical trench capacitor being formed from common material of a single deposition layer of conductive material.

23. An electronic device comprising:

a semiconductor substrate having a first side and a second side;

a plurality of trenches on the first side of the substrate, each of the trenches extending into the substrate from the first side;

conductive material lining each of the trenches;

a vertical interconnect that extends through the substrate from the first side to the second side, the vertical interconnect having walls;

a single deposition layer of dielectric material on the first and second sides of the substrate, on the conductive material lining each of the trenches, and on the walls of the vertical interconnect.

24. The electronic device of claim 23, wherein the vertical interconnect has a first part and a second part, the first part extending from the first side of the substrate to the second part, the second part extending from the second side of the substrate to the first part and being wider than the first part.

25. The electronic device of claim 23, wherein the vertical interconnect includes a plurality of parallel trenches.

26. The electronic device of claim 24, wherein the first part of the vertical interconnect includes a plurality of parallel trenches each of which extends from the first side of the substrate to the second part of the vertical interconnect.

27. The electronic device of claim 23, wherein the plurality of trenches form a vertical trench capacitor.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.